Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A method of aligning instructions in a processor comprising:

storing a plurality of instructions of different sizes in a plurality of buffer areas, each buffer area including a plurality of sub-buffers, each sub-buffer storing a unit instruction width, with an instruction of greater than a unit instruction width stored in more than one sub-buffer;

aligning a first instruction from said buffer areas;

decoding a size of the first instruction;

selecting at least one of said plurality of sub-buffers from which to output said first instruction on an output part;

during said outputting, determining a beginning of a second instruction from selected ones of the plurality of sub-buffers based on the size of the first instruction, decoding the size of the second instruction, and determining whether processing the second instruction will deplete any of said plurality of buffer areas based on comparing a most significant bit of a pointer to a first sub-buffer to a most significant bit of a pointer to a second sub-buffer; and

based on said determining whether processing the second instruction will deplete said plurality of buffer areas, instructing the plurality of buffer areas to receive additional instructions.

2-3. (Canceled)

4. (Previously Presented) The method of Claim 1, further comprising storing a first instruction across a plurality of sub-buffers prior to processing the instructions.

5. (Original) The method of Claim 1, further comprising adding the size of the first instruction to a current instruction position to determine the beginning of the second instruction.

6. (Previously Presented) The method of Claim 1, further comprising aligning ahead a number of cycles at least equal to a cache latency such that the determining whether processing the second instruction will deplete said plurality of buffer areas occurs at least said number of cycles before instructing the plurality of buffer areas to receive additional instructions.

7. (Original) The method of Claim 1, further comprising aligning instructions in a digital signal processor.

8. (Previously Presented) The method of Claim 1, further comprising issuing a request to a memory to reload the plurality of buffer areas.

9-18. (Canceled)

19. (Previously Presented) The processor of Claim 27, wherein the processor aligns ahead a number of cycles at least equal to a cache latency such that the predicting when at least one of the plurality of buffer areas will be empty occurs at least said number of cycles before sending a signal to instruct said at least one of the plurality of buffer areas to load additional instruction data.

20. (Previously Presented) The processor of Claim 27, wherein the processor is a digital signal processor.

21. (Previously Presented) An apparatus, including instructions residing on a machine-readable storage medium, for use in a machine system to align instructions in a processor, the instructions causing the machine to:

store a plurality of instructions of different sizes in a plurality of buffer areas, each buffer area including a plurality of sub-buffers, each sub-buffer storing a unit instruction width, with an instruction of greater than a unit instruction width stored in more than one sub-buffer;

decode a size of a first instruction from said plurality of buffer areas;

select at least one of said plurality of sub-buffers from which to output said first instruction on an output part;

during said outputting, determine a beginning of a second instruction from selected ones of the plurality of sub-buffers based on the size of the first instruction, decode the size of the second instruction, and determine whether processing the second instruction will deplete at least one of the plurality of buffer areas based on comparing a most significant bit of a pointer to a first sub-buffer to a most significant bit of a pointer to a second sub-buffer; and

based on said determining whether processing the second instruction will deplete the plurality of buffer areas, instruct the plurality of buffer areas to receive additional instructions.

22-23. (Canceled)

24. (Previously Presented) The apparatus of Claim 21, wherein a first instruction is stored across a plurality of sub-buffers prior to processing the instructions.

25. (Previously Presented) A method of processing instructions within a processor, comprising:

storing instructions of different widths within a cache having a plurality of buffer areas, each buffer area having a plurality of subportions, each subportion in the cache storing a unit instruction width, where an instruction of unit width takes up a single subportion in the cache, and an instruction of more than said unit width takes up more than one subportion within the cache;

multiplexing each of the subportions of said cache to an output point, and selecting contents of at least one of said cache subportions as a current instruction;

during said selecting said current instruction, predicting which of said buffer areas within said cache will be depleted of instruction data within a number of cycles approximately equal to

a latency of the cache based on comparing a most significant bit of a pointer to a first subportion to a most significant bit of a pointer to a second subportion, and instructing loading of the buffer areas that are predicted to be depleted with additional instruction data.

26. (Canceled)

27. (Previously Presented) A processor comprising:

a plurality of buffer areas, each buffer area adapted to store a plurality of instructions of different widths in a plurality of subparts, each of said subparts storing a unit instruction width, and said instructions of greater than a unit instruction width being stored in multiple said subparts;

a multiplexer, connected to said plurality of subparts, and selecting and aligning contents of at least one of said plurality of subparts from any of said subparts within said buffer areas as a current instruction; and

a predictor, operating to predict when at least one of the plurality of buffer areas will be empty based on comparing a most significant bit of a pointer to a first subpart to a most significant bit of a pointer of a second subpart, and to send a signal to instruct said at least one of the plurality of buffer areas to load additional instruction data.

28-31. (Canceled)